CLAIMS

What is claimed is:

1. A self-clocking memory device, comprising:

a memory array;

a memory input circuit operable to receive an input clock signal and generate a memory operation initiation signal in response thereto; and

a memory control circuit operable to receive the memory operation initiation signal and generate one or more control signals to initiate a memory operation in response thereto, the memory control circuit further operable to identify completion of the memory operation and generate a cycle ready strobe signal in response thereto,

wherein the memory input circuit receives the cycle ready strobe signal as an input and generates a next memory operation initiation signal in response thereto for initiation of a next memory operation.

2. The self-clocking memory device of claim 1, further comprising a bit line precharge circuit operable to precharge one or more bit lines of the memory array to a predetermined potential after a memory operation is completed in response to enabling a bit line precharge signal as one of the one or more control signals of the memory control circuit.

3. The self-clocking memory device of claim 2, wherein the memory control circuit further comprises a cycle ready circuit operable to generate the cycle ready strobe signal in response to the enabling of the bit line precharge signal.

4. The self-clocking memory device of claim 3, wherein the memory operation initiation signal comprises an internal memory clock signal operable to

disable the bit line precharge signal upon a transition thereof, thereby signaling an initiation of the memory operation.

5. The self-clocking memory device of claim 3, wherein the cycle ready circuit is further operable to generate the cycle ready strobe signal a predetermined period of time after the enabling of the bit line precharge signal.

6. The self-clocking memory device of claim 5, wherein the predetermined period of time is sufficient to ensure that the true and complement bit lines associated with a selected memory cell within the memory array are substantially equalized and have reached a predetermined voltage level.

7. The self-clocking memory device of claim 1, further comprising a tracking circuit operable to generate a reset signal a predetermined period of time after generation of the memory operation initiation signal, wherein the reset signal is operable to disable the memory operation initiation signal.

8. The self-clocking memory device of claim 7, wherein the predetermined period of time is sufficient to ensure the true and complement bit lines associated with a selected memory cell in the memory array establish a voltage differential based on a state of the selected memory cell.

9. The self-clocking memory device of claim 8, wherein the tracking circuit employs column or row address loading associated with the memory array to generate a delay substantially equal to the predetermined period of time.

10. A memory device, comprising:

a memory array; and

a memory control circuit operable to initiate a first memory operation based on an external system clock, and initiate a second memory operation based on an indication that the first memory operation is complete.

11. The memory device of claim 10, wherein the memory control circuit is operable to detect completion of the first memory operation and generate a cycle ready signal for initiation of the second memory operation.

12. The memory device of claim 11, wherein the memory control circuit is operable to generate the cycle ready signal a predetermined period of time after a bit line precharge signal is enabled, wherein the predetermined period of time is sufficient to ensure that true and complement bit lines associated with a selected memory cell substantially equalize and reach a predetermined value.

13. The memory device of claim 12, wherein a time period in which the true and complement bit lines associated with the selected memory cell substantially equalize and reach a predetermined value values and is a function of temperature, supply voltage or process variation, respectively, and wherein the memory control circuit is operable to vary the predetermined period of time associated with the generation of the cycle ready signal in accordance with variations in the time period for bit line equalization.

14. The memory device of claim 11, wherein the memory control circuit comprises an input multiplexer logic circuit operable to select one of a signal associated with the external system clock and the cycle ready signal and generate an internal cock signal in response thereto based on whether the memory device sin a burst mode of operation.

15. The memory device of claim 14, further comprising a bit line precharge circuit associated with the memory array, and operable to precharge true and complement bit lines associated with a selected memory cell in the memory array, and wherein the memory control circuit is operable to enable a bit line precharge signal to initiate a precharge of the true and complement bit lines via the bit line precharge circuit in response to the generated internal clock signal.

16. The memory device of claim 15, wherein the memory control circuit is further operable to disable the bit line precharge circuit based on another state of the internal clock signal.

17. The memory device of claim 16, wherein the memory control circuit further comprises a tracking circuit operable to generate a reset control signal a predetermined period of time after the internal cock signal disables the bit line precharge circuit, wherein the predetermined period of time is sufficient for the true and complement bit lines associated with the selected memory cell to establish a voltage differential therebetween based on a state of the selected memory cell.

18. The memory device of claim 17, further comprising a sense amp circuit associated with the memory array, wherein the tracking circuit is operable to generate a sense amp enable signal after generating the reset signal, thereby latching data associated with the selected memory cell via the sense amp circuit.

19. The memory device of claim 17, wherein the reset signal transitions the internal clock signal, thereby enabling the bit line precharge circuit for a next memory operation.

20. The memory device of claim 17, wherein the memory control circuit further comprises a cycle ready circuit operable to generate the cycle ready signal for initiation of the second memory operation based upon a transition of the bit line precharge signal indicating initiation of a precharge of true and complement bit lines associated with a selected memory cell within the memory array.

21. The memory device of claim 20, wherein the cycle ready circuit is operable to generate the cycle ready signal a predetermined period of time after the bit line precharge signal is enabled, wherein the predetermined period of time is sufficient to ensure that true and complement bit lines associated with a selected memory cell substantially equalize and reach a predetermined value.